AMENDMENTS TO THE SPECIFICATION

Please replace paragraph beginning at page 2, line 21, with the following amended paragraph:

Next, referring to FIG. 1b, a photoresist layer 22 covering the lower portion 18 of the trench 14 is formed. Subsequently, a sacrificial layer 20 covering the upper portion 16 of the trench 14 and the pad layer 12 is deposited. Then, referring to FIG. 1c, the photoresist layer 22 and the sacrificial layer 20 from the pad layer 12 are later removed by anisotropic etching. As a result, [[the]] a residual sacrificial layer [[20]] 21 is formed in the upper portion 16 of the trench 14.

Please replace paragraph beginning at page 3, line 1, with the following amended paragraph:

Finally, referring to FIG. 1d, the silicon substrate 10 uncovered by the residual sacrificial layer [[20]] 21 of the lower portion 18 of the trench 14 is etched by isotropic etching using ammonia and diluted hydrogen fluoride to form the lower portion 24 of the bottle-shaped trench [[14]] 17. The lower portion [[22]] 24 is wider (at width 15) than the upper portion 16 (at width 13).

Please replace paragraph beginning at page 6, line 28, with the following amended paragraph:

First, referring to FIG. 2a, a semiconductor substrate 100, such as a p-type silicon substrate or n-type silicon substrate is provided. Herein, use of the term substrate includes devices formed within a semiconductor wafer and the layers overlying the wafer. Next, a pad structure 102 is formed on the substrate 100. The pad structure 102 can comprise a pad oxide layer or a pad nitride layer, wherein the pad oxide layer can be formed on the substrate in advance, and a pad nitride layer formed on the pad oxide layer subsequently. Preferably, the pad oxide layer, such as silicon oxide with a thickness of 50Å to 300Å, is formed using thermal oxidation at ~~850-950C°~~ 850-950°C, APCVD, or LPCVD. The pad nitride layer such as silicon nitride with a thickness of 1000Å to 2000Å is formed using LPCVD at ~~750-800C°~~ 750-800°C, wherein $SiCl_2H_2$ and NH_3 are reactants.

Please replace paragraph beginning at page 7, line 14, with the following amended paragraph:

Subsequently, referring to FIG. 2b, a first hard mask layer ~~110~~ 109 is formed on the ~~ad~~ pad structure 102, and a second hard mask layer ~~112~~ 111 is formed on the first hard mask layer ~~110~~ 109. Next, a photoresist pattern 120 is formed on the second hard mask layer ~~112~~ 111 by photolithography. Suitable material for the first hard mask layer ~~110~~ 109 is silicide, such as boro phosphor silicate glass (BPSG), phosphor silicate glass (PSG), boro silicate glass (BSG), or arsenic silicate glass (AsSG). Preferably, the first hard mask layer ~~110~~ 109 of BSG with a thickness of 8000 to 15000Å, such as 13000Å, is formed by LPCVD, wherein SiH_4, BF_3, and B_2H_6 are reactants. Suitable material for the second hard mask layer ~~112~~ 111 is polysilicon or doped polysilicon. Preferably, the second hard mask layer ~~112~~ 111 of polysilicon with a thickness of 500 to 5000Å is formed by LPCVD at ~~500-650C°~~ 500-650°C with doped ion concentration between 1E20 to 1E21 atoms/cm^3, wherein PH_3, SiH_4, and N_2 are reactants. The thickness of the second hard mask layer ~~112~~ 111 can be 3000Å in this embodiment.

Please replace paragraph beginning at page 8, line 3, with the following amended paragraph:

Subsequently, referring to FIG. 2c, the second hard mask layer ~~112~~ 111 is etched anisotropically with the photoresist pattern 120 acting as a mask, to form a first opening 130 and expose the first hard mask layer ~~110~~ 109. Preferably, the anisotropic etching process can be MERIE, ECR or RIE with reactants comprising SF_6, O_2, Cl_2, HBr, or a combination thereof.

Please replace paragraph beginning at page 8, line 10, with the following amended paragraph:

Subsequently, referring to FIG. 2d, the photoresist pattern 120 is removed, and a spacer layer 124 formed conformally on the first hard mask layer ~~110~~ 109 and the etched second hard mask layer 112 and in the first opening 130. Suitable material for the spacer layer 124 is dielectric material such as silicon nitride, and the spacer layer 124 can be formed by a method such as LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Please replace paragraph beginning at page 8, line 18, with the following amended paragraph:

Subsequently, referring to FIG. 2e, the spacer layer 124 is etched anisotropically, for example as RIE, to remove the spacer layer 124 from the etched second hard mask layer 112

and ~~a part of the~~ an etched spacer layer ~~124~~ 124' is formed into the first opening 130 to form a second opening 132, by a self-aligned etching step resulting in a precise scale of the second opening 132.

Please replace paragraph beginning at page 8, line 25, with the following amended paragraph:

Subsequently, referring to FIG. 2f, a third hard mask layer 114 is formed on the above structure to fill the second opening 132. Herein, the third hard mask layer 114 can be subjected to a flattening process to remove the part of the third hard mask layer 114 ~~from~~ outside the second opening 132. Suitable materials for third hard mask layer 114 and second hard mask layer ~~112~~ 111 can be the same or different. Furthermore, the materials of third hard mask layer 114 and the second hard mask layer ~~112~~ 111 are different from those of the first hard mask layer ~~110~~ 109. The suitable material of the third hard mask layer 114 can be polysilicon. Preferably, the third hard mask layer 114 of polysilicon is formed by LPCVD at ~~500-650C°~~ 500-650°C. In addition, the flattening process can be chemical mechanical polishing.

Please replace paragraph beginning at page 9, line 9, with the following amended paragraph:

Subsequently, referring to FIG. 2g, the etched spacer layer ~~124~~ 124' is removed completely by, for example a hot phosphoric acid solution, to expose the first hard mask layer ~~110~~ 109. Next, referring to FIG. 2h, the first hard mask layer ~~110~~ 109 is ~~and the substrate 100 are~~ etched to expose a third opening 134 with a salient 110a of the etched first hard mask layer 110, with the etched second hard mask layer 112 and the third hard mask layer 114 acting as masks. Next, the etched second hard mask layer 112 and the third hard mask layer 114 are removed.

Please replace paragraph beginning at page 9, line 18, with the following amended paragraph:

Subsequently, referring to FIG. 2i, the salient 110a of the etched first hard mask layer 110, the etched first hard mask layer 110, and the substrate 100 are etched to remove the salient 110a of the etched first hard mask layer 110 completely, with the etched first hard mask layer 110 beyond the third opening 134 acting as a sacrifice layer to protect the substrate 100 under the etched first hard mask layer 110, resulting in a doughnut-shaped hollow 136 in the substrate 100 formed by etching of the substrate 100. When the salient 110a is removed completely by ~~etchimg~~ etching, the etched first hard mask layer 110 beyond the third opening

134 is etched to form a residual first hard mask layer 110b simultaneously, due to salient 110a having a higher etching rate than the etched first hard mask layer 110. Furthermore, the pad structure 102 is etched to form a first etched pad structure 102a.

Please replace paragraph beginning at page 10, line 3, with the following amended paragraph:

Subsequently, referring to FIG. 2j, the doughnut-shaped hollow 136 of the substrate ~~110~~ 100 and the first etched pad structure ~~102~~ 102a are etched by anisotropic etching such as RIE, with the residual first hard mask layer 110b acting as a mask, to form the geometric deep trench 138 and a second etched pad structure 102b. Moreover, an additional sacrificial layer can be formed on the residual first hard mask layer 110b to maintain the entire sacrificial layer, comprising the residual first hard mask layer 110b and the additional sacrificial layer, has a thickness sufficient to protect the substrate 100 during the etching of the doughnut-shaped hollow 136 of the substrate ~~110~~ 100.